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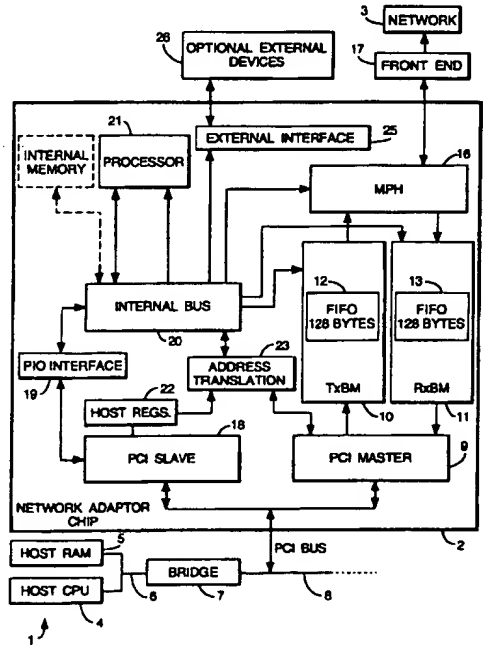
(54) Communication network end station and adaptor card

(57) A communication network end station comprises a host device (1) including a processor (4) and a memory (5); a bus (8); and a communication network interface device (2) connected to the host device via the bus and, in use, to a communication network (3) along which data is transmitted in accordance with a network protocol. The communication network interface device includes processing means (10,11) for transferring data to and from the network in accordance with the network protocol. The control code for operating the processing means is stored in the host device memory (5). The processing means is adapted to route incoming data and associated network protocol information, as it is received, to the host device memory (5). The bus (8) is capable of transmitting data and associated network protocol information at a speed compatible with the operating speed of the communication network.

Fig.1.



EP 0 789 302 A1

Description

The invention relates to a communication network end station for use with a communication network and also to an adaptor card for insertion into such a communication network end station.

Typically, network adaptor cards contain a RAM buffer store to facilitate data transfer from the network to the host system and vice versa. This RAM is used as temporary local storage for data destined for transmission to the network or just received from the network. The adaptor card processor has high speed access to this storage with a guaranteed minimum rate of transfer which is essential for proper operation of the network.

Transfer between the RAM buffer store and the host system may be implemented in a variety of ways, the most common being: i) shared memory, where all or part of the RAM buffer store is accessible to both the adaptor and the host, ii) programmed input/output where the adaptor card processor transfers data using I/O cycles to a fixed location, which then map to an auto-incrementing location in the buffer store, iii) DMA transfers, where a DMA engine, either on the adaptor card or in the host, transfers data from the adaptor card store to the host memory and vice versa without intervention from the adaptor card processor.

Typical token ring network adaptor cards contain an on-board processor to manage network status and control signalling (MAC frames in token ring), and to schedule the flow of data to and from the network. The processor runs instructions stored in on-board ROM, or downloaded into on-board RAM when the system starts up.

There is a continuing need to reduce the cost of adaptor cards.

In accordance with one aspect of the present invention, a communication network end station comprises a host device including a processor and a memory; a bus; and a communication network interface device connected to the host device via the bus and, in use, to a communication network along which data is transmitted in accordance with a network protocol, the communication network interface device including processing means for transferring data to and from the network in accordance with the network protocol and is characterised in that the control code for operating the processing means is stored in the host device memory; in that the processing means is adapted to route incoming data and associated network protocol information, as it is received, to the host device memory; and in that the bus is capable of transmitting data and associated network protocol information at a speed compatible with the operating speed of the communication network.

In accordance with a second aspect of the present invention, an adaptor card for use with a communication network end station comprising a host device including a processor and a memory, and a bus to which the adaptor card is connected in use, wherein the bus is capable of transmitting data and associated network protocol information at a speed compatible with the operating speed of the communication network the adaptor card includes a communication network interface device having processing means for transferring data to and from the network in accordance with the network protocol and is characterised in that the control code for operating the processing means is stored in the host device memory in use; and in that the processing means is adapted to route incoming data and associated network protocol information, as it is received, to the host device memory.

We have designed a new interface device, preferably in the form of an adaptor card, in which the need for on-board RAM storage is overcome. This is achieved by storing not only incoming data in the host memory but also associated network protocol information (for example token ring MAC frames) and the control code for operating the processing means. This latter feature means that even on-board ROM is avoided although a very small amount of ROM or RAM may be provided for holding code corresponding to the idle state of the processing means, (i.e. the state where frames are passed from the host to the network and from the network to the host without modification by the processor; the code required to generate and process MAC frames being stored in host memory).

Preferably, the bus comprises one of a PCI, EISA, and Microchannel bus. These provide high data transfer rates.

In use, part of the memory map for the processing means is mapped into addresses in the host memory, those addresses being secured against reuse by the host operating system.

Typically, the interface device further includes a direct memory access (DMA) device for transferring information to and from the host device memory via the bus. The use of a DMA device reduces the complexity of the operations performed by the processing means and leads to very fast transfers of data between the host device and interface device.

In some cases, the interface device may further include a pair of FIFOs, one of which receives information from the communication network prior to transfer to the host memory device and the other of which receives information for transmission onto the communication network from the host memory device. The use of FIFOs absorbs the effect of small delays in transfer to and from the host device.

An example of a communication network end station according to the present invention will now be described with reference to Figure 1 which is a schematic block diagram of the end station.

The end station comprises a host device 1 connected to an adaptor card 2 which provides an interface between the host device 1 and a communication network 3, such as a token ring. The host device 1 includes a host CPU 4 and host RAM 5 linked by a high speed proprietary bus 6. The bus 6 is linked by an interface bridge 7 to a PCI bus 8 which is linked to the adaptor

card 2.

The adaptor card 2 includes a PCI master unit 9 providing a DMA engine, the unit 9 being connected to respective transmit and receive buffer managers 10,11. Each buffer manager 10,11 contains a respective FIFO 12,13. The buffer managers 10,11 are connected to a protocol handler 16 described in more detail in our co-pending International Patent Application No. PCT/GB 96/02058 incorporated herein by reference. The protocol handler 16 is connected to front end circuitry 17 of conventional form which provides a link to the network 3.

The PCI bus 8 is also connected to a PCI slave unit 18 which is linked via a PIO interface 19 to an internal bus 20. An on-board processor 21 is connected to the internal bus 20, as is a memory address translation unit 23. The PCI slave 18 is also connected a set of registers 22. An external interface 25 is connected to the internal bus 20 and is used to connect to optional external devices 26. The transmit buffer manager 10 and the receive buffer manager 11 can be controlled via the internal bus 20.

The PIO 19 interface allows the host processor to access devices attached to the internal bus without the intervention of the on-board processor.

An overview of the operation of the end station shown in Figure 1 will now be described. Firstly, it will be noted that there is virtually no memory provided on the adaptor card 2. The code for running the processor 21 is stored in the host RAM 5 while frames being received and transmitted are also stored in the RAM 5 including protocol control frames such as MAC frames. MAC frames may be stored in different locations corresponding to high and low priority frames respectively. The buses 6,8 can be operated sufficiently fast to enable the code and frames to be transferred between the host and the adaptor card without compromising operation of the network.

Data received from the network

When data is received on the network 3, it is passed to the front end circuit 17 where it is demodulated and passed to the protocol handler 16. The protocol handler 16 passes frames destined for its own unique adaptor address to the receive buffer manager 11.

In addition, the buffer manager 11 notifies the processor 21, via the internal shared bus 20, the type of received frame, i.e. MAC or data (LLC). Copying of the frame will stop if address match fail is signalled or there is insufficient space to store the frame in host memory.

The receive buffer manager 11 in conjunction with the DMA engine In the PCI master unit 9 writes the frame from the FIFO 13 into the host RAM 5.

The buffer manager 11 ensures that the received frame is correctly reported to the rest of the network as having been copied if, and only if, there was sufficient space available in the host RAM buffers to store the entire packet.

If the FIFO 13 overflows because access to bus 8 is not granted, by the interface 7, the copied bit in the incoming frame will not be set.

Data to be transmitted onto network

When the host CPU 4 signals to the transmit buffer manager 10 that there is a data packet ready for transmission, the buffer manager begins reading data from the host RAM 5 using the DMA engine within the master unit 9. This data is transferred into the FIFO 12 and when a predetermined amount of data has been placed there, the buffer manager 10 instructs the protocol handler 16 to acquire a free token from the network 3. When the token has been obtained, data is removed from the FIFO 12 and serialised onto the network by the protocol handler 16. As the FIFO empties, the transmit buffer manager 10 ensures that there is always sufficient data available for transmission to continue until the end of the frame. The buffer manager 10 automatically reads linked buffers and data fragments from the host memory 5 until it encounters a flag indicating the end of the frame.

Processing of MAC frames

The function of the processor 21 is to process and generate network management packets and to initiate transmission of data stored in the host memory. The processor 21 gains access to the host memory 5 through the address translation unit 23, which is controlled by a bank of base registers within the host register block 22. These are initialised by the host processor 4 when the network driver software is started. The driver must allocate one or more continuous blocks of host physical memory and lock them so that they are removed from any memory management scheme running on the host. The driver can then set the base registers in the network adaptor card 2 to point to this physical memory area. Within the adaptor card 2, each base register maps up to 64K bytes of the processor memory space.

MAC (network management) packets are automatically written into a receive buffer area in the host memory 5 by the receive buffer manager 11.

In some cases, the receive buffer manager 11 will distinguish between different types of MAC frame and high priority MAC frames will be stored in a different location from low priority frames.

Claims

1. A communication network end station comprising a host device (1) including a processor (4) and a memory (5); a bus (8); and a communication network interface device (2) connected to the host device via the bus and, in use, to a communication network (3) along which data is transmitted in

accordance with a network protocol, the communication network interface device including processing means (10,11) for transferring data to and from the network in accordance with the network protocol characterised in that the control code for operating the processing means is stored in the host device memory (5); in that the processing means is adapted to route incoming data and associated network protocol information, as it is received, to the host device memory (5); and in that the bus (8) is capable of transmitting data and associated network protocol information at a speed compatible with the operating speed of the communication network.

2. An end station according to claim 1, wherein the bus comprises one of a PCI, Eisa, and Microchannel bus.

3. An end station according to claim 1 or claim 2, wherein the interface device (2) further includes a direct memory access (DMA) device for transferring information to and from the host device memory via the bus.

4. An end station according to any of the preceding claims, wherein the interface device (2) further includes a pair of FIFOs (12,13), one of which receives information from the communication network prior to transfer to the host memory device and the other of which receives information for transmission onto the communication network from the host memory device.

5. An end station according to any of the preceding claims, wherein the communication network protocol is a Token Ring protocol.

6. A communication network connected to at least one end station according to any of the preceding claims.

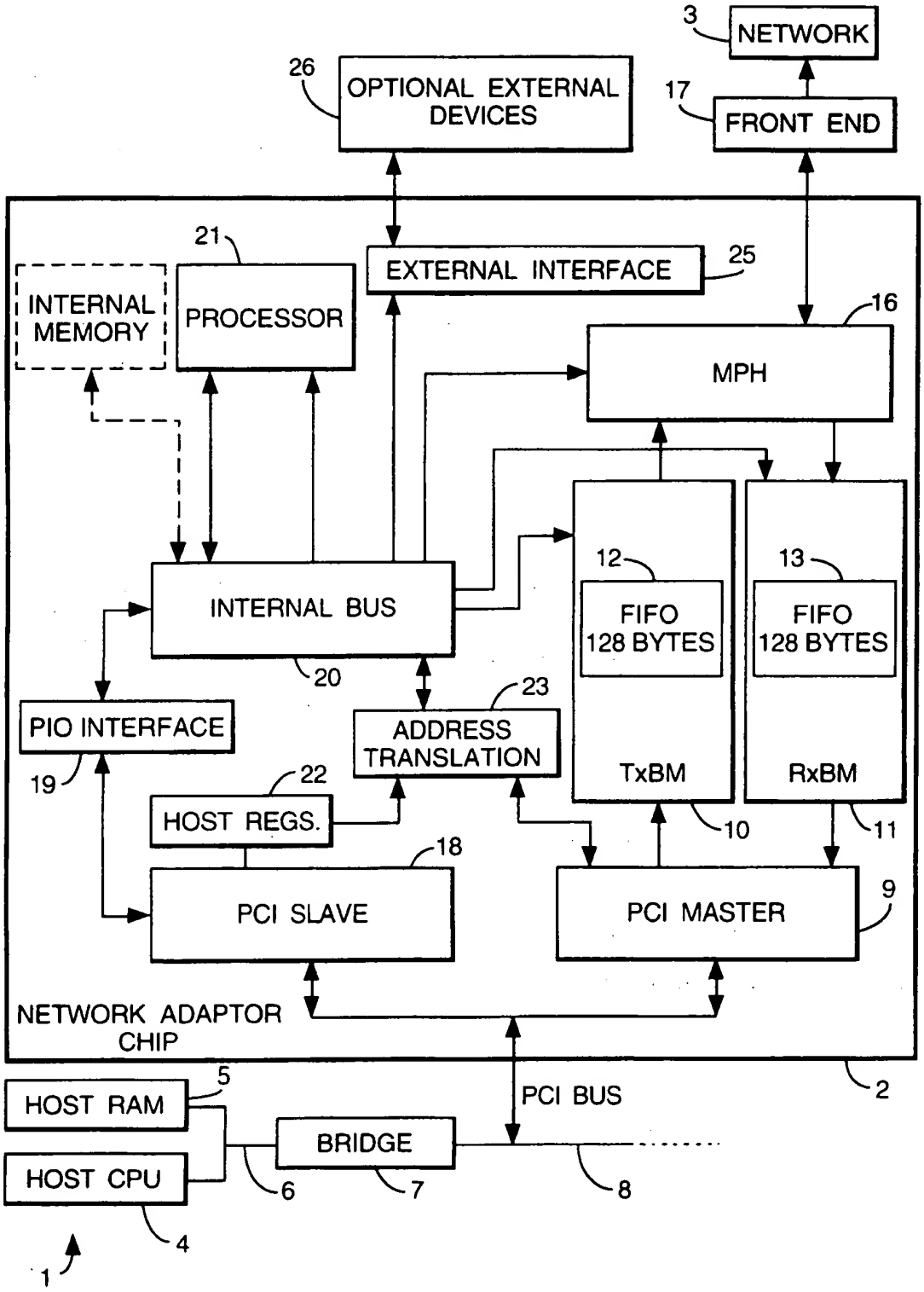
7. An adaptor card for use with a communication network end station comprising a host device (1) including a processor (4) and a memory (5), and a bus (8) to which the adaptor card is connected in use, wherein the bus is capable of transmitting data and associated network protocol information at a speed compatible with the operating speed of the communication network, the adaptor card including a communication network interface device (2) having processing means (10,11) for transferring data to and from the network in accordance with the network protocol characterised in that the control code for operating the processing means is stored in the host device memory in use; and in that the processing means is adapted to route incoming data and associated network protocol information, as it is received, to the host device memory.

8. An adaptor card according to claim 7, further including a direct memory access (DMA) device for transferring information to and from the host device memory via the bus.

9. An adaptor card according to claim 7 or claim 8, further including a pair of FIFOs (12,13), one of which receives information from the communication network prior to transfer to the host memory device and the other of which receives information for transmission onto the communication network from the host memory device.

10. A communication network end station according to any of claims 1 to 5, wherein the interface device is contained in an adaptor card according to any of claims 7 to 9.

Fig.1.


3
NETWORK
26
OPTIONAL EXTERNAL DEVICES
17
FRONT END
21
INTERNAL MEMORY
PROCESSOR
EXTERNAL INTERFACE
25
16
MPH
12
13
FIFO 128 BYTES
FIFO 128 BYTES
INTERNAL BUS
20
23
PIO INTERFACE
19
ADDRESS TRANSLATION
TxBM
RxBM
22
HOST REGS.
10
11
18
PCI SLAVE
PCI MASTER
9
NETWORK ADAPTOR CHIP
2
5
HOST RAM
PCI BUS
BRIDGE
HOST CPU
6
7
8
4
1

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 96 30 9157

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP 0 657 824 A (AMD) * page 2, line 49 - line 58 * * page 4, line 25 - page 6, line 18; figure 3 *	1-10	G06F13/12
A	EP 0 577 115 A (3COM) * page 4, column 3, line 35 - page 5, column 5, line 3; figures 1,2 *	1-10	
A	ELECTRONICS , vol. 61, no. 16, October 1988, NEW YORK US, page 139 XP000009682 T. MANUEL: "Here's One Net No Computer Can Outrun" * page 139, right-hand column, paragraph 2 - paragraph 4; figure *	1,3,4, 6-10	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 May 1997	Gill, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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